ABSTRACT OF THE DISCLOSURE

A system and method for waiving a verification check associated with a circuit design. In one embodiment, a first engine integrates waiver options associated with the circuit design's design objects into a hierarchical verification tree having the verification check. Responsive to a verification check violation, a second engine traverses a portion of the hierarchical verification tree to determine a list of applicable waivers. A third engine resolves the list of applicable waivers to determine the disposition of the verification check violation.